Amendments to the Drawings:

Replacement copies of Figs. 2B and 3C are attached. The amendments to the drawings correct the deficiencies noted in the Office Action.

Attachments: Replacement Sheets for FIGS. 2B and 3C.

REMARKS

In the non-final Office Action, the Examiner objected to the drawings, rejected claims 39-64 and 72 under 35 U.S.C. § 112, first paragraph as allegedly not being enabled by the disclosure, rejected claims 39-41, 45-50, 53, 54, 57-60, 63-68, and 71 under 35 U.S.C. § 103(a) as being unpatentable over MUNTER et al. (U.S. Patent No. 5,126,999) in view of MORRISSEY et al. (U.S. Patent No. 5,463,762); and rejected claims 42-44, 51, 52, 55, 56, 61, 62, 69, 70, and 72 under 35 U.S.C. § 103(a) as unpatentable over MUNTER et al. in view of MORRISSEY et al. and further in view of SUZUKI (U.S. Patent No. 4,799,215).

By this Amendment, Applicants have amended the drawings to overcome the Examiner's objections. Applicants have amended claim 49 to improve form and canceled claim 50 without prejudice or disclaimer. Accordingly, claims 39-49 and 51-72 are now pending in the present application.

Initially, the Examiner objected to the drawings for allegedly incorrectly identifying several elements in Figs. 2B and 3C. Accordingly, Applicants have amended these figures to correct the noted errors. It should be noted that, although the Examiner suggested re-designating element Bi of Fig. 3C as element "270", Applicant has determined that a label of "302" is more suitable to disclosure of Fig. 3C. Applicants request reconsideration and withdrawal of the pending drawing objections.

Rejections under 35 U.S.C. § 112

Claims 39-64 were rejected under 35 U.S.C. § 112, first paragraph for allegedly failing to

include all features that are essential or critical to the practice of the invention. More specifically, the Examiner requests that each element of input interface 300, packing queue 380 and in-line packet processing device 386 be included within each claim. Applicants respectfully traverse.

35 U.S.C. § 112, first paragraph requires that "[t]he specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

§ 2164.08(c) of the M.P.E.P. recites:

> A feature which is **taught as critical in a specification** and is not recited in the claims should result in a rejection of such claim under the enablement provision section of 35 U.S.C. § 112. In determining whether an unclaimed feature is critical, the entire disclosure must be considered. Features which are merely preferred are not to be considered critical. In re Goffe, 542 F.2d 564, 567, 191 USPQ 429, 431 (CCPA 1976).
>
> Limiting an applicant to the preferred materials in the absence of limiting prior art would not serve the constitutional purpose of promoting the progress in the useful arts. Therefore, an enablement rejection based on the grounds that a disclosed critical limitation is missing from a claim should be made only when the language of the specification makes it clear that the limitation is critical for the invention to function as intended. Broad language in the disclosure, including the abstract, omitting an allegedly critical feature, tends to rebut the argument of criticality.

Although various specificities regarding illustrative and exemplary embodiments of the claimed invention are set forth in the specification and drawings of the present application, none of the non-claimed elements are described as "critical" or "essential" to the operation of the invention. In fact, language supportive of the scope of the pending claims may be found at various places in the specification, such as page. 16, lines 13-28 and pg. 17, lines 14-22. As

recited above, enablement rejections based on the grounds that a disclosed critical limitation is missing from a claim should be made **only when the language of the specification makes it clear that the limitation is critical for the invention to function as intended**. Clearly, no suck language appears in the present application. Accordingly, reconsideration and withdrawal of the rejection under 35 U.S.C. § 112, first paragraph are respectfully requested.

Rejections under 35 U.S.C. § 103(a)

Claims 39-41, 45-50, 53, 54, 57-60, 63-68, and 71 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over MUNTER et al. in view of MORRISSEY et al. Applicants respectfully traverse the rejection.

A proper rejection under 35 U.S.C. § 103 requires that three basic criteria be met. First, there must be some suggestion or motivation, either in the references themselves, or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest each and every claim limitation. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not the applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The cited combination of MUNTER et al. and MORRISSEY et al. fail to disclose or reasonably suggest the combination of features recited in claims 39, 41, 45-50, 53, 54, 57-60, 63-66, and 71.

Claim 39, for example, is directed to an apparatus for processing packets. The apparatus comprises a first input queue configured to receive a stream of incoming packets and to output

beginning portions of packets as the beginning portions are received without waiting for the respective packets to be received in their entirety; a first in-line packet processor for receiving the beginning portions from the first input queue, each beginning portion including first header information, and for detecting the existence of an error in the first header information of each beginning portion; and a first memory for storing packets received at the first input queue and for which the first in-line packet processor did not detect an error in the corresponding first header information.

The cited combination of MUNTER et al. and MORRISSEY et al. do not disclose or suggest the combination of features recited in claim 39. For example, neither MUNTER et al. nor MORRISSEY et al. disclose or suggest a first memory for storing packets received at the first input queue and *for which the first in-line packet processor did not detect an error in the corresponding first header information*.

The Examiner alleged that item 40 in MUNTER et al. corresponds to the above-recited features of claim 39 (Office Action, page 4). Applicants respectfully disagree.

In the Office Action, the Examiner identified item 41 (header decoder) and item 43 (error detector) of MUNTER et al. as allegedly corresponding to the first in-line packet processor and item 40 (input FIFO RAM buffer) of MUNTER et al. as allegedly corresponding to the first memory (Office Action, pp. 3-4). Even assuming, for the sake of argument, that header decoder 41 and error detector 43 could be equated to the first in-line packet processor and buffer 40 can be equated to the first memory (points that Applicants do not concede), nowhere does MUNTER et al. disclose or suggest that either header decoder 41 or error detector 43 generates a signal to drop a packet **before the packet is stored in buffer 40** and for which the first in-line packet

processor did not detect an error in the corresponding first header information, as required by claim 39.

In fact, MUNTER et al. specifically teaches against this feature of claim 39. MUNTER et al. discloses:

> **As a data packet is being written into a FIFO**, an error detector 43 is calculating its own check byte for the entire packet. As the packet ends, the locally calculated check byte is compared to the one received from the header and the faulty packet is discarded upon non-coincidence and the FIFO's write pointer is reset to the last byte of the previous packet address.

(col. 5, line 67 - col. 6, line 6). In this section, MUNTER et al. discloses that the packet is written into the FIFO (of buffer 40) and if the locally calculated check byte does not match the one in the header of the packet, then the packet is discarded from the FIFO. This is directly contrary to generating a signal to drop a packet before the packet is stored in buffer 40 and for which it detects an error in the corresponding first header information, as recited in claim 39.

The disclosure of MORRISSEY et al. does not remedy this deficiency in the disclosure of MUNTER et al. For at least this reason claim 39 is patentable over the cited combination of MUNTER et al. and MORRISSEY et al.

Claims 41 and 45-48 depend from claim 39 and are therefore patentable over the combination of MUNTER et al. and MORRISSEY et al. for at least the reasons given above, with respect to claim 39. Moreover, claims 41 and 45-58 recited additional features neither disclosed nor suggested by the combination of MUNTER et al. and MORRISSEY et al.

For example, claim 41 recites that the first in-line packet processor generates a signal to drop a packet before the packet is stored in the first memory and for which it detects an error in the corresponding first header information. MUNTER et al. does not disclose or suggest the

combination of features recited in claim 41.

As indicated above, the Examiner identified item 41 and item 43 (error detector) of MUNTER et al. as allegedly corresponding to the first in-line packet processor and item 40 (buffer) of MUNTER et al. as allegedly corresponding to the first memory (Office Action, pp. 3-4). Even assuming, for the sake of argument, that header decoder 41 and error detector 43 could be equated to the first in-line packet processor and buffer 40 can be equated to the first memory (points that Applicants do not concede), nowhere does MUNTER et al. disclose or suggest that either header decoder 41 or error detector 43 generates a signal to drop a packet **before** the packet is stored in buffer 40 and for which it detects an error in the corresponding first header information, as would be required by claim 41. As discussed in detail above, MUNTER et al. specifically teaches against the features of claim 41.

For at least these additional reasons, Applicants submit that claim 41 is patentable over the combination of MUNTER et al. and MORRISSEY et al.

Independent claim 49, as amended, is directed to a device for processing packets. The device comprises an input queue for receiving a stream of packets and for outputting beginning portions of packets as the beginning portions are received without waiting for the respective packets to be received in their entirety; a header processor configured to receive the beginning portions from the input queue, each beginning portion including first header information, for detecting the existence of an error in the first header information included in each beginning portion, wherein upon detecting the existence of an error in a first header information, the header processor generates an error signal indicating that the corresponding packet contains an error; and a buffer manager for causing each packet received at the input queue to be stored in memory

if the buffer manager does not receive an error signal corresponding to the packet from the header processor.

MUNTER et al. and MORRISSEY et al. do not disclose or suggest the combination of features recited in claim 49. For example, neither MUNTER et al. nor MORRISSEY et al. disclose or suggest a buffer manager for causing each packet received at the input queue to be stored in memory if the buffer manager does not receive an error signal corresponding to the packet from the header processor.

Although not specifically referenced, the Examiner alleged that item 40 in MUNTER et al. corresponds to the memory recited in claim 49 (Office Action, page 4). Applicants respectfully disagree for at least reasons similar to the reasons given with regard to claim 39.

For at least these reasons, Applicants submit that claim 49, as amended, is patentable over the combination of MUNTER et al. and MORRISSEY et al.

Independent claim 53 recites features similar to, but potentially different in scope from, claim 49. Accordingly, claim 53 is patentable over the combination of MUNTER et al. and MORRISSEY et al. for at least reasons similar to those set forth above, with respect to claim 49.

Claims 54, 57, and 58 depend from claim 53 and are, therefore, patentable over MUNTER et al. and MORRISSEY et al. for at least the reasons given with regard to claim 53.

Independent claim 59 recites features similar to, but potentially different in scope from, claim 49. Accordingly, claim 59 is patentable over the combination of MUNTER et al. and MORRISSEY et al. for at least reasons similar to those set forth above, with respect to claim 49.

Claims 60, 63, and 64 depend from claim 59 and are, therefore, patentable over the combination of MUNTER et al. and MORRISSEY et al. for at least the reasons given with regard to claim 59.

Independent claim 65 recites features similar to, but potentially different in scope from, claim 49. Accordingly, claim 65 is patentable over the combination of MUNTER et al. and MORRISSEY et al. for at least reasons similar to those set forth above, with respect to claim 49. As discussed in detail above, MUNTER et al. does not disclose or suggest detecting the existence of an error in the beginning portion while the remaining portions of the packet are being received, as recited in claim 65. Instead, MUNTER et al. clearly discloses detecting a faulty packet after the packet is stored in the FIFO (col. 5, line 67 - col. 6, line 6). For at least these reasons, Applicants submit that claim 65 is patentable over MUNTER et al. and MORRISSEY et al. Claims 66 and 71 depend from claim 65 and are, therefore, patentable over MUNTER et al. and MORRISSEY et al. for at least the reasons given with regard to claim 65.

For at least the foregoing reasons, Applicants respectfully request the reconsideration and withdrawal of the rejection of claims 39, 41, 45-49, 53, 54, 57-60, 63-66, and 71 under 35 U.S.C. § 103(a) based on MUNTER et al. in view of MORRISSEY et al.

Claims 42-44, 51, 52, 55, 56, 61, 62, 69, 70, and 72 were rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over MUNTER et al. in view of MORRISSEY et al. and further in view of SUZUKI. Applicants respectfully traverse the rejection.

Claims 42-44 and 72 depend from claim 39, claims 51 and 52 depend from claim 49, claims 55 and 56 depend from claim 53, claims 61 and 62 depend from claim 59, and claims 69 and 70 depend from claim 65. Without acquiescing in the Examiner's rejection, Applicants respectfully submit that the disclosure of SUZUKI does not cure the deficiencies in the disclosures of MUNTER et al. and MORRISSEY et al. identified above with regard to claims 39, 49, 53, 59, and 65. Therefore, claims 42-44, 51, 52, 55, 56, 61, 62, 69, 70, and 72 are patentable

over MUNTER et al., MORRISSEY et al., and SUZUKI, whether taken alone or in any reasonable combination, for at least the reasons given with regard to claims 39, 49, 53, 59, and 65.

For at least the foregoing reasons, Applicants respectfully request the reconsideration and withdrawal of the rejection of claims 42-44, 51, 52, 55, 56, 61, 62, 69, 70, and 72 under 35 U.S.C. § 103 based on MUNTER et al., MORRISSEY et al., and SUZUKI.

If the Examiner does not believe that all pending claims are now in condition for allowance, the Examiner is urged to contact the undersigned to expedite prosecution of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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